BEE 332 Devices and Circuits II
Spring 2017
Lab 4: Multi-stage amplifiers*

1 Objectives

The objectives of this experiment are to examine the characteristics of several multi-stage amplifier configurations. Several of these will be breadboarded and measured for voltage gain, frequency response and signal swing.

In addition to the performance measurements, notice how the biasing of each amplifier stage is achieved, how the signal is coupled from stage to stage, and what design strategy has been adopted to desensitize the amplifier performance to variations in the transistor parameters.

For each amplifier in this experiment, try to answer the question: "What has been achieved by connecting the transistors in this configuration?" To begin to answer this question, first identify whether a particular transistor is providing bias stabilization for other transistors or is a gain stage in the signal path. Some transistors may simultaneously function in both roles.

Then try to determine what components set the voltage gain of the amplifier. Track the path of the signal through the different stages of the amplifier and try to understand how much voltage gain is produced across each stage, how big the signal is at each node along the path, and what limits the signal swing at each node. Mark up a copy of the schematic to show the DC bias voltage at each node, the path that the signal takes from input to output, and anything else that is of interest to you.

The amplifier circuits described in this experiment are not as simple as those previously used in this lab. While all of the component values are fairly close to the values needed to make the circuits work, normal variations in transistor parameters may require that each amplifier circuit be "tuned-up" slightly to center the signal swings or trim out the gain. This is left for you to do without any explicit instructions and is intended to force you to understand how the circuits work and to gain skill in electronic troubleshooting.

2 Circuits

Here are the circuits you'll be experimenting with in this lab. The final circuit is very similar to what you'll need for your design project.

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* This lab was originally designed by R. B. Darling and has been revised by T. Chen and N. Hamilton.

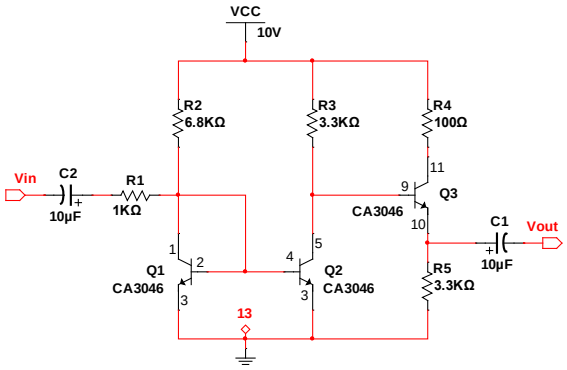

Figure 1. Wideband CE-EF amplifier.

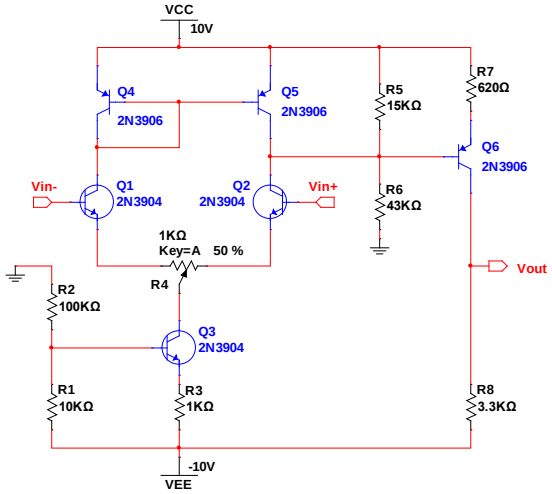

Figure 2. A simple opamp.

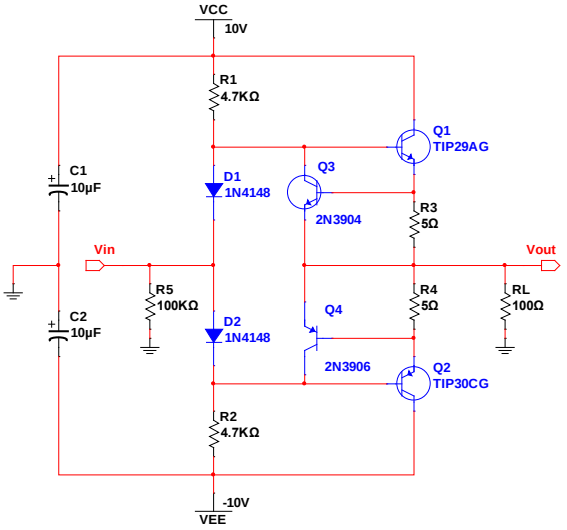

Figure 3. Complementary class AB output stage.

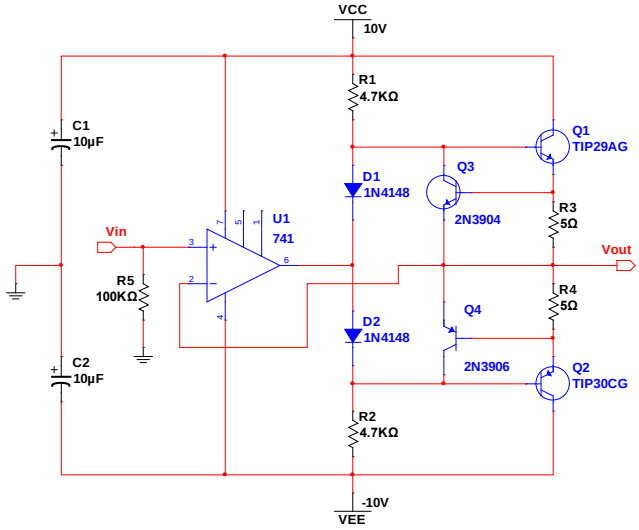

Figure 4. Multi-stage amplifier with feedback.

3 Wideband CE-EF amplifier

A common-emitter (CE) stage is one of the most widely used BJT configurations for obtaining both voltage and current gain. However, its gain is proportional to the resistance on its collector. Attaching a heavy load (low resistance) will thus reduce the gain. One simple means for improving on this is to buffer the output voltage with an emitter-follower (EF) stage, also known as a common-collector stage.

3.1 Circuit

Build the circuit in figure 5 (same as figure 1.)

Record the measured values of your resistors and the quiescent collector, base and emitter voltages of each of the transistors.

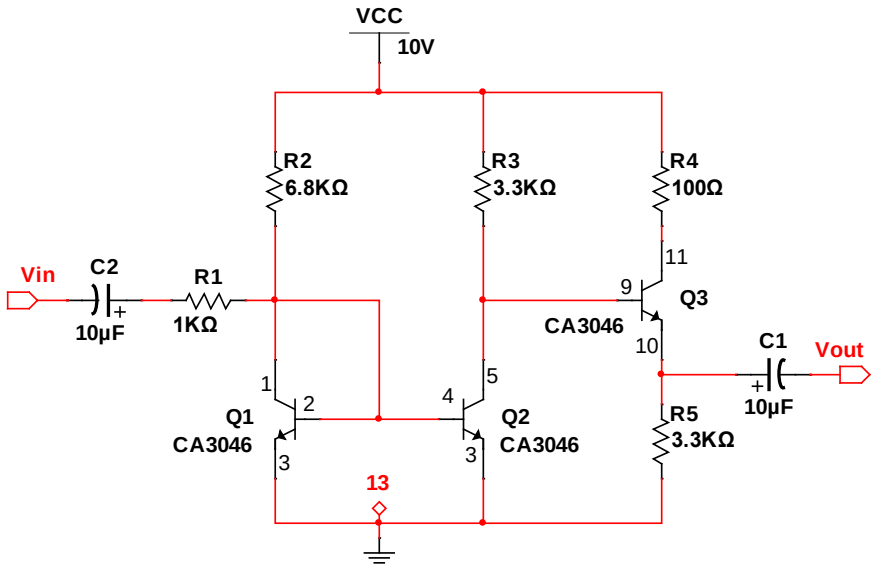

Figure 5. Wideband CE-EF amplifier.

3.2 Measurements

1. Set Vin = 1 Vpp, 1.0 KHz sine wave, 0 V DC offset.
2. Capture an oscilloscope screenshot with:
   a. DC coupling with Vin on channel 1 and Vout on channel 2.
   b. On-screen measurements of Vpp for Vin and Vout, frequency for Vin, and mean for Vout.
   c. Cursors at the peaks on Vout.
3. Calculate Av.
4. Increase the frequency of Vin until Av has fallen by 3 dB. Capture a screenshot with the same on-screen measurements as before and calculate Av.
5. Reset Vin to 1.0 KHz and increase the amplitude until Vout begins clipping on either peak. Capture a screenshot with the same on-screen measurements as before.
6. Continue increasing the amplitude of Vin until Vout begins clipping on the other peak. Capture a screenshot with the same on-screen measurements as before.

3.3 Analysis

1. Explain how the Q1-Q2 pair sets the bias level for Q3.
2. Explain why Av is approximately given by R3/R1.
3. Explain what sets the clipping levels for this amplifier.

4 An active load: A simple opamp

An active load usually refers to the use of a transistor's output characteristics (IC versus VCE) to provide a high output resistance but at a much larger level of DC current than what a passive resistor alone could provide. Using an active load for a common-emitter stage

greatly increases the voltage gain since the collector resistance for the CE amplifier stage is now the output resistance of the active load transistor.

4.1 Circuit

Build the circuit in figure 6 (same as figure 2).

Record the measured values of your resistors and the quiescent collector, base and emitter voltages of each of the transistors.

In this circuit, an active load is used on both collector legs of an *npn* differential pair. When connected like a current mirror as shown, the pair of active loads also has the benefit of routing both sides of the differential signal into the next stage, the base of Q6. The active loads in this case form a differential to single-ended converter.

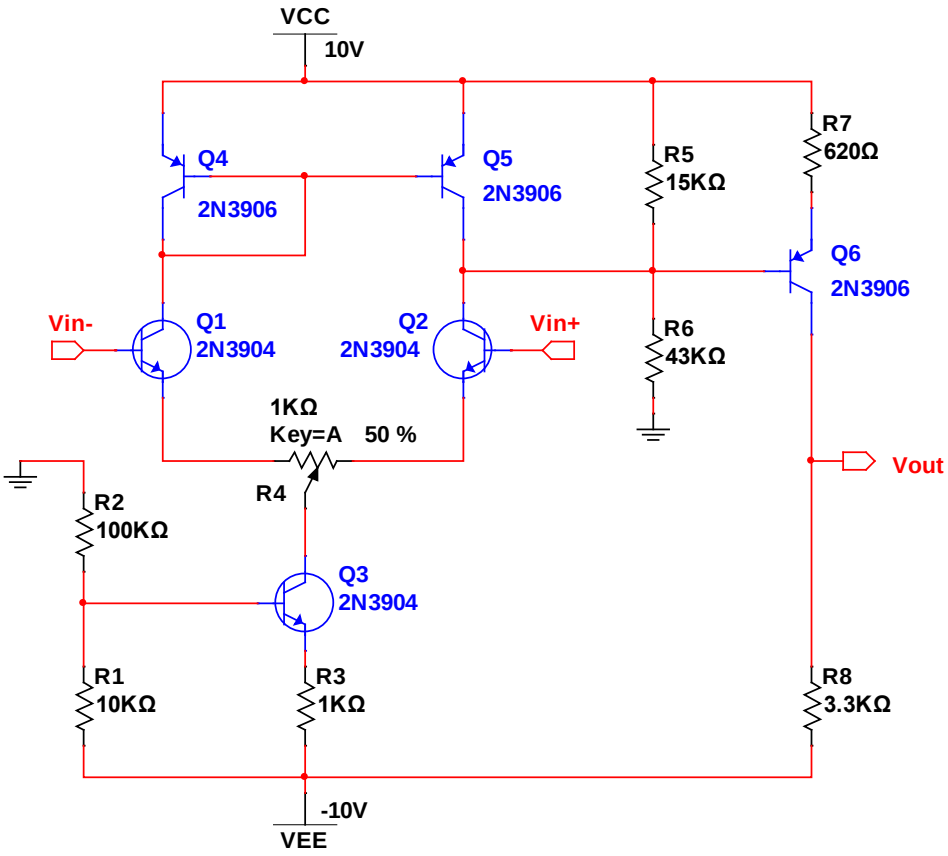

Figure 6. A simple opamp.

Transistor Q3 provides an improved current source for the differential pair which greatly increases the common-mode rejection ratio.

Transistor Q6 implements a simple common-emitter stage with a load resistor of R8. This adds some final gain and current drive to the output pin. Resistors R5, R6 and R7 provide bias stabilization for the output stage.

R4 is a trimpot between the emitters of Q1 and Q2. This will lower the voltage gain of this stage slightly, but it will allow the input differential amplifier to be balanced to help bias the circuit so that the output voltage will be about zero when the differential input voltage is also zero.

4.2 Measurements

1. Trim the circuit by grounding both Vin+ and Vin–, then adjusting the trimpot to set Vout = 0 V.
2. Ground Vin– and set Vin+ = 100 mVpp, 1 KHz sine wave, 0 V DC offset. This is differential mode with an unbalanced input. Capture a screenshot with the same on-screen measurements as before. Calculate Av.
3. Increase the frequency of Vin+ until Av has fallen by 3 dB. Capture a screenshot with the same on-screen measurements as before and calculate Av.
4. Reset Vin+ to 1.0 KHz and increase the amplitude until Vout begins clipping on either peak. Capture a screenshot with the same on-screen measurements as before.
5. Continue increasing the amplitude of Vin until Vout begins clipping on the other peak. Capture a screenshot with the same on-screen measurements as before.
6. Set Vin– = Vin+ = 10 Vpp, 1.0 KHz sine wave, 0 V DC offset. This is common mode. Capture a screenshot as before and calculate Av.

4.3 Analysis

1. Calculate the differential-mode voltage gain of the amplifier in dB.
2. Calculate the common-mode voltage gain of the amplifier in dB.
3. Calculate the common-mode rejection ratio (CMRR) for this amplifier in dB.
4. Explain what determines the clipping voltage levels.

5 Complementary class-AB output stage

Emitter followers (or common-collector) stages were shown to be a nice means for increasing the output current level of an amplifier and buffering voltage gain stages. However, when a large bias current runs continuously through such a stage, it dissipates far more power than it delivers to the load, resulting in poor power efficiency.

One way to correct this is to only operate the transistor when it is delivering current to the load, termed class-AB operation. Using two transistors of opposite sex but driven by the same input signal is termed a complementary output stage and provides a power efficient configuration for output buffering or current boosting. This circuit can be used to boost the output current of an opamp. Putting the output stage inside the feedback loop causes the gain of the opamp to linearize the characteristics of the output stage.

5.1 Circuit

Build the circuit in figure 7 (same as figure 3). Use heat sinks on Q1 and Q2.

Record the measured values of your resistors and the quiescent collector, base and emitter voltages of each of the transistors.

In this circuit, Q3 and Q4 act as short-circuit protection. If the output is shorted, the currents through R3 and R4 will rise and so will the voltages at the bases of Q3 and Q4. Once they turn on, VB1 and VB2 will drop, turning those transistors off.

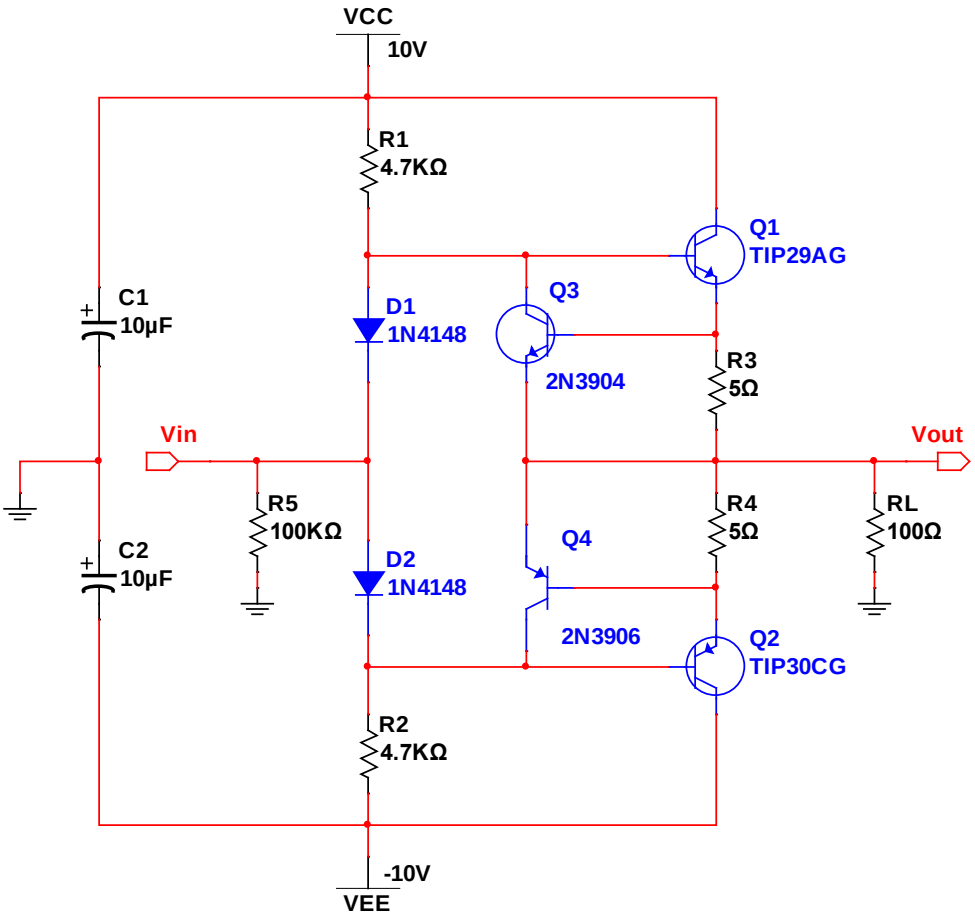

Figure 7. A simple opamp.

5.2 Measurements

1. Set Vin = 5.0 Vpp, 1.0 kHz. Capture a screenshot with the same on-screen measurements as before and calculate Av.
2. Increase the frequency of Vin until Av has fallen by 3 dB. Capture a screenshot with the same on-screen measurements as before and calculate Av.
3. Reset Vin to 1.0 KHz and increase the amplitude until Vout begins clipping on either peak. Capture a screenshot with the same on-screen measurements as before.
4. Continue increasing the amplitude of Vin until Vout begins clipping on the other peak. Capture a screenshot with the same on-screen measurements as before.

5.3 Analysis

1. Calculate the voltage gain for this output stage.
2. Comment on any distortion that is seen in the output voltage waveform.
3. Calculate the output current that will cause the short-circuit protection to become active.
4. If clipping happens on one peak before the other, explain how the circuit might be trimmed with a potentiometer instead of one of the resistors.

6 Multi-stage amplifier with feedback

6.1 Circuit

Modify the AB amplifier circuit to add an opamp front-end and a negative feedback loop as shown in figure 8 (same as figure 4).

Record the measured values of your resistors and the quiescent collector, base and emitter voltages of each of the transistors.

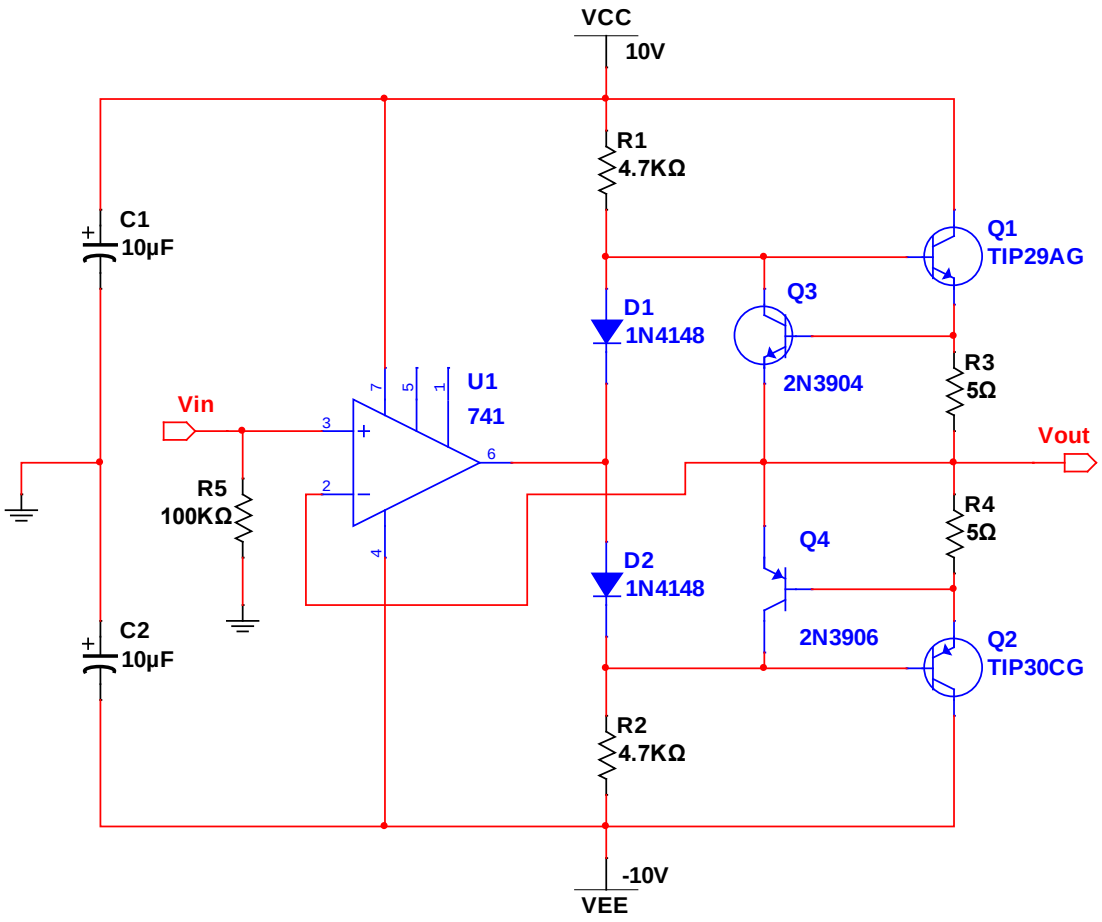

Figure 8. Multi-stage amplifier with feedback.

6.2 Measurements

1. Set Vin = 5.0 Vpp, 1.0 kHz. Capture a screenshot with the same on-screen measurements as before and calculate Av.
2. Increase the frequency of Vin until Av has fallen by 3 dB. Capture a screenshot with the same on-screen measurements as before and calculate Av.

3. Reset Vin to 1.0 KHz and increase the amplitude until Vout begins clipping on either peak. Capture a screenshot with the same on-screen measurements as before.
4. Continue increasing the amplitude of Vin until Vout begins clipping on the other peak. Capture a screenshot with the same on-screen measurements as before.

6.3 Analysis

1. Compare the clipping levels and bandwidth of the circuit to that of the output stage without the opamp.
2. Compare the distortion of the opamp circuit to that of the output stage without the opamp. What are the tradeoffs?